## REMARKS

A typographical error in a paragraph of the specification has been corrected.

Typographical errors have been corrected in claims 6 and 20, claim 17 has been amended to recite the limitation of claim 5 rather than duplicate one of the limitations of claims 11, 13 and 15, and claims 21-36 have been added. Claims 1-36 remain in the application.

The Examiner rejected claims 1-8 under 35 USC §102(e) as being anticipated by Pham and rejected claims 9-20 under 35 USC §103(a) as being unpatentable over Pham.

An enclosed Declaration of co-inventor Rodney Dean Miller presents schematics (Exhibits 1-4), a 46-page layout verification and archive signoff (Exhibit 5), and a 14-page test summary (Exhibit 6) which are all dated prior to the September 15, 2003 filing date of Pham.

As detailed in the Declaration, the schematics show a phase-locked loop (PLL) system (Exhibit 1), a VCO in the PLL system (Exhibit 2), a VCO stage (Exhibit 3) and a controller in the PLL system (Exhibit 4). Exhibits 1-4 include all elements and their arrangements that are shown in FIGS. 1-6 of Applicants' application and that are recited in Applicants' claims 1-20. The Declaration particularly points out the correlation between elements and arrangements of the schematics and elements and arrangements of Applicants' claims 1-20.

In addition, the layout verification and archive signoff (Exhibit 5) confirms the readiness of the design for mask production and archive and shows that all fabrication details for the elements of the schematics were completed prior to Pham's September 15, 2003 filing date. Finally, the test results (Exhibit 6) show that 1125 tests were conducted on 388 flat panel display interfaces that each included the system shown in Exhibits 1-4. Failures were only found in device tests that did not concern the phase-locked loop system.

In accordance with 37CFR§1.131, the enclosed Declaration establishes reduction to practice of the claimed invention prior to Pham's filing date so that Pham is not a valid reference under either of 35 USC §102(e) or 35 USC §103(a) and claims 1-20 are now in condition for allowance.

Additional claims 21-36 have been added to patentably distinguish over Pham in case the subject matter of Pham is prior art under some other basis presently unknown to Applicants.

Added claims 21-26 are supported by the filed specification and drawings and are directed to an inverter system which includes inverters coupled in a ring wherein inverter current in each of the inverters is a function of a loop control voltage and a time constant of each of the inverters is a function of a command signal that changes when the control voltage exits a predetermined control-voltage range. The ring is shown in Applicants' FIG. 4 and time constants are disclosed in the filed specification (e.g., in the paragraph that begins at line 26 of page 8).

Applicant notes that Pham fails to teach and claim a ring of inverters, fails to teach and claim a feedback loop that alters an inverter current, and fails to teach and claim the alteration of inverter time constants when a control voltage exits a predetermined control-voltage range.

Added claims 27-32 are supported by the filed specification and drawings and are directed to an inverter system which includes inverters coupled in a ring wherein inverter current in each of the inverters is a function of a loop control voltage and a function of a command signal that changes when the control voltage exits a predetermined control-voltage range. Structure for altering each inverter's current in response to a command signal is shown in FIG. 5C and disclosed in the filed specification (e.g., in the paragraph that begins at line 17 of page 9).

Applicant notes that Pham fails to teach and claim a ring of inverters, fails to teach and claim a feedback loop that alters an inverter current, and fails to teach and claim the alteration of the inverter current when a control voltage exits a predetermined control-voltage range.

Added claims 33-36 are supported by the filed specification and drawings and are directed to an inverter system which includes inverters and switches coupled in a ring wherein inverter current in each of the inverters is a function of a loop control voltage and the switches alter the loop in response to a command signal that changes when the control voltage exits a predetermined

control-voltage range. The ring and switches (73) are shown in FIG. 4 and disclosed in the filed specification (e.g., in the paragraph that begins at line 5 of page 8).

Applicant notes that Pham fails to teach and claim a ring formed with inverters and switches and fails to teach and claim a controller that commands the switches to thereby alter the number of inverters in the ring when a control voltage exits a predetermined control-voltage range.

Applicant further notes that Pham teaches away from the limitations discussed above because he teaches VCOs formed with resonant LC tank circuits (e.g., see lines 20-24 of column 4 and lines 8-15 of column 10) and tuning varactors (e.g., see lines 27-28 of column 4 and lines 27-29 of column 10) which Applicants do not employ.

Added claims 21-36 thus patentably distinguish over the cited art so that claims 1-36 are now in condition for allowance.

Applicants therefore request reconsideration and withdrawal of the rejections and an early allowance of claims 1-36.

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